SECTION III—REMARKS

This amendment is submitted in response to the Office Action mailed August 23, 2006. Claims 1, 12 and 34 are amended, and claims 1-22 and 34-44 remain pending in the application. Applicants respectfully request reconsideration of the application and allowance of all pending claims in view of the above amendments and the following remarks.

Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 1-22 and 34-44 under 35 U.S.C § 103(a) as obvious in view of, and therefore unpatentable over, U.S. Patent No. 6,780,772 to Uzoh *et al.* ("*Uzoh*") in view of U.S. Patent Application Publication No. 2004/0072423 to Jorne *et al.* ("*Jorne*") and further in view of U.S. Patent No. 6,764,713 to Wytman ("*Wytman*").

Applicants respectfully traverse the Examiner's rejections. To establish a *prima* facie case of obviousness, the Examiner must establish that three criteria are met: (1) the prior art references must teach or suggest all the claim limitations; (2) some suggestion or motivation to combine the references must be found in the prior art; and (3) there must be a reasonable expectation of success. MPEP § 2143. For at least the reasons explained below, Applicants respectfully submit that the Examiner has not established a *prima facie* case of obviousness.

Claim 1, as amended, recites a process combination including:

providing a wafer comprising an inter-layer dielectric (ILD) having a feature therein, an under-layer deposited on

the ILD, a barrier layer deposited on the under-layer and a conductive layer deposited on the barrier layer;

exposing the barrier layer;

immersing the wafer in an electrolyte, such that at least the barrier layer is wholly immersed in the electrolyte;

applying an electrical potential between the wafer and an electrode immersed in the electrolyte until the underlayer is exposed in the field surrounding the feature; and

removing the under-layer from the field surrounding the feature using selective etching or gentle chemicalmechanical polishing.

(italics added). The Examiner alleges that *Uzoh* discloses the recited method substantially as claimed, but lacks anticipation only because it does not disclose the process details recited in the claim. Specifically, the Examiner concedes that *Uzoh* does not disclose: (1) that the wafer is placed in a holder that seals the edges thereof; and (2) that the wafer is placed in an electrolyte, such that at least the barrier layer is immersed in the electrolyte and that an electrical potential is applied between the wafer and an electrode immersed in the electrolyte until at least part of the barrier layer is removed. To make up for these deficiencies in *Uzoh* the Examiner cites *Jorne* for its alleged disclosure of an electrolytic solution and an applied voltage, and cites *Wytman* for its alleged disclosure of an apparatus which can be used for electropolishing techniques and which seals the edges

of the wafers. The Examiner concludes that it would have been obvious at the time the present invention was made to combine *Uzoh* and *Jorne* to arrive at the present invention.

Applicants respectfully disagree. *Uzoh* discloses that:

In other embodiments of this invention, it may be desirable to electropolish the metal layer 206 down to the barrier layer 208. A portion of the barrier layer 208 may then be removed, as shown in FIG. 8, by, for example, a very brief reactive ion etching (RIE) process stopping on the insulator layer 210. Barrier layers 208 such as TaN, Ta, tungsten (W) and their various compounds can be removed with a suitable fluoride plasma, such as CF₄ plasma. The barrier layer 208 may also be removed by, for example, using an abrasive slurry, electropolishing, or wet etching.

(column 8, lines 50-59). *Uzoh* discloses that metal layer 206 is electropolished down to barrier layer 208 and discloses, with reference to figure 8, that "a portion of the barrier layer" can be removed with reactive ion etching. Figure 8 clearly shows that the entire barrier layer in the field outside feature 204 is gone. The "portion of the barrier layer" referred to in the text must therefore refer to the entire barrier layer outside feature 204, not some portion of the thickness of barrier layer 208 or some layer within a multi-layer barrier layer 208. *Uzoh* therefore teaches that the entire barrier layer 208—whether made up of a single layer or multiple layers—should be removed using only a single method chosen from among those mentioned.

Nowhere does *Uzoh* disclose, teach or suggest that different methods should be used to remove different layers within the barrier layer. *Uzoh* therefore cannot disclose, teach or suggest a process combination including "applying an electrical potential between the wafer and an electrode immersed in the electrolyte until the under-layer is exposed in the field surrounding the feature" and "removing the under-layer from the field surrounding the feature using selective etching or gentle chemical-mechanical polishing." *Jorne* and *Wytman* similarly do not disclose, nor does the Examiner allege that they disclose, the recited process. When combined *Uzoh*, *Jorne*, and *Wytman* therefore cannot disclose, teach or suggest the recited process combination. Applicants submit that *Uzoh*, *Jorne* and *Wytman* therefore cannot obviate the claim and respectfully request withdrawal of the rejection and allowance of the claim.

Regarding claims 2-11, if an independent claim is non-obvious under 35 U.S.C. § 103, then any claim depending therefrom is also non-obvious. MPEP § 2143.03; *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). As discussed above, claim 1 is in condition for allowance. Applicants submit that claims 2-11 are therefore also allowable by virtue of their dependence on an allowable independent claim, as well as by virtue of the features recited therein. Applicants therefore respectfully request withdrawal of the rejections and allowance of these claims.

Claim 12, as amended, recites a process combination including:

providing a wafer comprising an inter-layer dielectric (ILD) having a feature therein, an under-layer deposited on

the ILD, and a barrier layer deposited on the under-layer, and a conductive layer deposited in the feature;

immersing the wafer in an electrolyte, such that at least the barrier layer is wholly immersed in the electrolyte;

applying an electrical potential between the wafer and an electrode immersed in the electrolyte until the underlayer is exposed in the field surrounding the feature; and

removing the under-layer from the field surrounding the feature using selective etching or gentle chemicalmechanical polishing.

(italics added). By analogy to the discussion above for claim 1, *Uzoh*, *Jorne* and *Wytman*, when combined, do not disclose, teach or suggest a combination including the recited limitations. Applicants submit that the combination of *Uzoh*, *Jorne* and *Wytman* therefore cannot obviate claim 12 and respectfully request withdrawal of the rejection and allowance of the claim.

Regarding claims 13-22, if an independent claim is non-obvious under 35 U.S.C. § 103, then any claim depending therefrom is also non-obvious. MPEP § 2143.03; *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). As discussed above, claim 12 is in condition for allowance. Applicants submit that claims 13-22 are therefore also allowable by virtue of their dependence on an allowable independent claim, as well as by virtue of the features recited therein. Applicants therefore respectfully request withdrawal of the rejections and allowance of these claims.

Claim 34, as amended, recites a process combination including:

providing a wafer comprising an inter-layer dielectric (ILD) having a feature therein, an under-layer deposited on the ILD, a barrier layer deposited on the under-layer and a conductive layer deposited on the barrier layer;

exposing the barrier layer;

placing the wafer in a holder that seals the edges thereof, such that, when the holder and the wafer are immersed in an electrolyte, the electrolyte will only affect a surface of the wafer;

immersing the holder and the wafer in the electrolyte, such that at least the barrier layer is wholly immersed in the electrolyte;

exposing the under-layer in the field surrounding the feature by electrolytically removing the barrier layer from the field surrounding the feature; and

removing the under-layer from the field surrounding the feature using selective etching or gentle chemicalmechanical polishing.

(italics added). By analogy to the discussion above for claim 1, *Uzoh*, *Jorne* and *Wytman*, when combined, do not disclose, teach or suggest a combination including the recited limitations. Applicants submit that the combination of *Uzoh*, *Jorne* and

Wytman therefore cannot obviate claim 34, and respectfully request withdrawal of the rejection and allowance of the claim.

Regarding claims 35-44, if an independent claim is non-obvious under 35 U.S.C. § 103, then any claim depending therefrom is also non-obvious. MPEP § 2143.03; *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). As discussed above, claim 34 is in condition for allowance. Applicants submit that claims 35-44 are therefore also allowable by virtue of their dependence on an allowable independent claim, as well as by virtue of the features recited therein. Applicants therefore respectfully request withdrawal of the rejections and allowance of these claims.

Conclusion

Given the above amendments and accompanying remarks, all claims pending in the application are in condition for allowance. If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to allowance of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 292-8600.

Charge Deposit Account

Please charge our Deposit Account No. 02-2666 for any additional fee(s) that may be due in this matter, and please credit the same deposit account for any overpayment.

Respectfully submitted,

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